What is claimed is:

1. A semiconductor device comprising:

a plurality of conductive patterns, each conductive pattern including a conductive layer and a capping layer stacked on an insulating layer disposed on a semiconductor substrate;

a first interlayer insulating layer filling at least one space between at least two adjacent conductive patterns and having a height whereby when disposed on the insulating layer, a top surface of the first interlayer insulating layer is lower than a top surface of the capping layer and higher than a top surface of the conductive layer;

a first spacer disposed on the first interlayer insulating layer and surrounding an outer surface of the capping layer;

a second interlayer insulating layer covering the first interlayer insulating layer, the capping layer, and the first spacer and having a planarized top surface; and

a contact plug passing through the second interlayer insulating layer, the first interlayer insulating layer, and the insulating layer, wherein the contact plug is positioned between the at least two conductive patterns, is electrically connected to the semiconductor substrate, has an outerwall surrounded by a second spacer, and is self-aligned with the capping layer.

2. The semiconductor device of claim 1, wherein the insulating layer, the first interlayer insulating layer, and the second interlayer insulating layer are formed of silicon oxide, and the capping layer, the first spacer, and the second spacer are formed of silicon nitride.

3. The semiconductor device of claim 1, wherein a width of the conductive layer is approximately 90 nm, a width of the top surface of the contact plug including the second spacer is approximately 120 nm, a width of the second spacer is approximately 300 Å, a height of the first spacer is approximately 500 Å, and a width of the first spacer is within the range of 200 – 300 Å.

4. The semiconductor device of claim 1, wherein the conductive layer is a bitline, and the contact plug is a storage node contact plug connecting a storage electrode with one of a cell pad connected to the semiconductor substrate and the semiconductor substrate.

5. The semiconductor device of claim 1, wherein the top surface and a bottom surface of the first interlayer insulating layer are flat.

6. The semiconductor device of claim 1, wherein the top surface of the first interlayer insulating layer has a V shape, and a bottom surface of the first spacer contacting the top surface of the first interlayer insulating layer is inclined.

7. The semiconductor device of claim 1, wherein the second spacer contacts the conductive layer.

8. A method of fabricating a semiconductor device comprising:

forming conductive patterns by depositing a conductive layer and a capping layer on an insulating layer disposed on a semiconductor substrate;

filling at least one space between at least two adjacent conductive patterns by depositing a first interlayer insulating layer in the at least one space;

exposing a part of a sidewall of the capping layer by wet etching the first interlayer insulating layer without damaging the capping layer;

forming a first spacer on an exposed part of the sidewall of the capping layer;

forming a second interlayer insulating layer on the first interlayer insulating layer, the capping layer and the first spacer, and planarizing a top surface of the second interlayer insulating layer;

forming a contact hole between the at least two adjacent conductive patterns, wherein the contact hole is self-aligned with the capping layer, by dry etching the second interlayer insulating layer, the first interlayer insulating layer, and the insulating layer;

forming a second spacer in an innerwall of the contact hole; and

forming a contact plug electrically connected to the semiconductor substrate by filling the contact hole with conductive material.

9. The method of claim 8, wherein when the first interlayer insulating layer is wet etched, a top surface of the conductive layer is not exposed.

10. The method of claim 8, wherein the insulating layer, the first interlayer insulating layer, and the second interlayer insulating layer are formed of silicon oxide, and the capping layer, the first spacer, and the second spacer are formed of silicon nitride.

11. The method of claim 8, wherein the first spacer is removed by the dry etching.

12. The method of claim 8, wherein a width of the conductive layer is approximately 90 nm, a width of the top surface of the contact pluginclude the second spacer is approximately 120 nm, a width of the second spacer is approximately 300 Å, a height of the first spacer is approximately 500 Å, and a width of the first spacer is within the range of 200 – 300 Å.

13. The method of claim 8, wherein the first spacer is completely removed when the contact hole is formed.

14. The method of claim 8, wherein a sidewall of the conductive layer is exposed when the contact hole is formed.

15. The method of claim 8, wherein the first spacer and the second spacer are formed by performing anisotropic plasma etching.

16. The method of claim 8, further comprising:

filling an entire space between the at least two adjacent conductive patterns by depositing the first interlayer insulating layer in the entire space; and

planarizing the first interlayer insulating layer and using the capping layer as a planarization stopper.

17. The method of claim 8, further comprising forming a surface of the first interlayer insulating layer in a V shape by depositing the first interlayer insulating layer using high-density plasma-chemical vapor deposition.

18. A semiconductor device comprising:

a plurality of conductive patterns, each conductive pattern including a conductive layer and a capping layer stacked on an insulating layer disposed on a semiconductor substrate;

a first interlayer insulating layer filling at least one space between at least two adjacent conductive patterns and having a height whereby when disposed on the insulating layer, a top surface of the first interlayer insulating layer is lower than a top surface of the capping layer and higher than a top surface of the conductive layer;

a first spacer disposed on the first interlayer insulating layer and surrounding an outer surface of the capping layer;

a second interlayer insulating layer covering the first interlayer insulating layer, the capping layer, and the first spacer; and

a contact plug passing through the second interlayer insulating layer, the first interlayer insulating layer, and the insulating layer, wherein the contact plug is positioned between the at least two conductive patterns and is self-aligned with the capping layer.

19. The semiconductor device of claim 18, wherein the contact plug includes an outerwall surrounded by a second spacer.

20. A method of fabricating a semiconductor device comprising:

forming conductive patterns by depositing a conductive layer and a capping layer on an insulating layer disposed on a semiconductor substrate;

filling at least one space between at least two adjacent conductive patterns with a first interlayer insulating layer;

exposing a part of a sidewall of the capping layer by wet etching the first interlayer insulating layer;

forming a first spacer on an exposed part of the sidewall of the capping layer;

forming a second interlayer insulating layer on the first interlayer insulating layer, the capping layer and the first spacer; and

forming a contact hole between the at least two adjacent conductive patterns, wherein the contact hole is self-aligned with the capping layer.

21. The method of claim 20, further comprising forming a second spacer in an innerwall of the contact hole.